IN THE CLAIMS

Please amend the claims as follows:

1. (Cancelled)

2. (Cancelled)

3. (Previously Presented) A method for transferring data in a network processing device, comprising:

reading a current entry in a receive memory;

identifying a time slot period for receiving the data according to the current entry in the receive memory;

identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

receiving data for the identified time slot period into the identified current receive channel register;

moving the current entry to a next entry in the receive memory when the time slot period expires;

identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

receiving data into the identified next receive channel register for the identified next time slot period; and

waiting for a next synchronization pulse before shifting data into the receive channel register associated with the beginning entry.

4. (Currently amended) A method for transferring data in a network processing device, comprising:

reading a current entry in a receive memory;

identifying a time slot period for receiving the data according to the current entry in the receive memory;

identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

receiving data for the identified time slot period into the identified current receive channel register;

moving the current entry to a next entry in the receive memory when the time slot period expires;

identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

receiving data into the identified next receive channel register for the identified next time slot period; and

moving to a beginning entry in the receive memory whenever a synchronization pulse is detected.

5. (Previously presented) A method for transferring data in a network processing device, comprising:

reading a current entry in a receive memory;

identifying a time slot period for receiving the data according to the current entry in the receive memory;

identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

receiving data for the identified time slot period into the identified current receive channel register;

moving the current entry to a next entry in the receive memory when the time slot period expires;

identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

receiving data into the identified next receive channel register for the identified next time slot period;

reading a current entry in a transmit memory;

identifying a time slot period for transmitting the data according to the current entry in the transmit memory;

identifying a current transmit channel register in the network processing device according to the current entry in the transmit memory;

transmitting data for the identified time slot period out from the identified current transmit channel register;

moving to a next entry in the transmit memory when the time slot period expires;

identifying a next time slot period and a next transmit channel register according to the next entry in the transmit memory; and

transmitting data out from the identified next transmit channel register for the identified next time slot period.

6. (Original) A method according to claim 5 including moving to a beginning entry in the transmit memory when a last entry is identified in the transmit memory and the time slot period expires.

7. (Original) A method according to claim 6 including waiting for a next synchronization pulse before writing data into the transmit channel register identified by the beginning entry.

8. (Original) A method according to claim 5 including moving to a beginning entry in the transmit memory whenever a synchronization pulse is detected.

9. (Original) A method according to claim 5 including loading different entries into the receive memory and transmit memory according a TDM data stream format used for transmitting and receiving the data.

10. (Original) A method according to claim 5 including reading the receive memory and receiving data into the receive channel registers and reading the transmit memory and transmitting data out from the transmit channel registers at the same.

11. (Currently amended) A system for transferring data in a network processing device, comprising:

means for reading a current entry in a receive memory;

means for identifying a time slot period for receiving the data according to the current entry in the receive memory;

means for identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

means for receiving data for the identified time slot period into the identified current receive channel register;

means for moving the current entry to a next entry in the receive memory when the time slot period expires;

means for identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

means for receiving data into the identified next receive channel register for the identified next time slot period; and

means for moving to another entry in the receive memory according to a detected synchronization pulse.

12. (Original) A system according to claim 11 including means for moving to a beginning entry in the receive memory when a last entry is identified in the receive memory and the time slot period expires.

13. (Previously presented) A system for transferring data in a network processing device, comprising:

means for reading a current entry in a receive memory;

means for identifying a time slot period for receiving the data according to the current entry in the receive memory;

means for identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

means for receiving data for the identified time slot period into the identified current receive channel register;

means for moving the current entry to a next entry in the receive memory when the time slot period expires;

means for identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

means for receiving data into the identified next receive channel register for the identified next time slot period; and

means for waiting for a next synchronization pulse before shifting data into the receive channel register associated with the beginning entry.

14. (Previously presented) A system for transferring data in a network processing device, comprising:

means for reading a current entry in a receive memory;

means for identifying a time slot period for receiving the data according to the current entry in the receive memory;

means for identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

means for receiving data for the identified time slot period into the identified current receive channel register;

means for moving the current entry to a next entry in the receive memory when the time slot period expires;

means for identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

means for receiving data into the identified next receive channel register for the identified next time slot period; and

means for moving to a beginning entry in the receive memory whenever a synchronization pulse is detected.

15. (Previously presented) A system for transferring data in a network processing device, comprising:

means for reading a current entry in a receive memory;

means for identifying a time slot period for receiving the data according to the current entry in the receive memory;

means for identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

means for receiving data for the identified time slot period into the identified current receive channel register;

means for moving the current entry to a next entry in the receive memory when the time slot period expires;

means for identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

means for receiving data into the identified next receive channel register for the identified next time slot period;

means for reading a current entry in a transmit memory;

means for identifying a time slot period for transmitting the data according to the current entry in the transmit memory;

means for identifying a current transmit channel register in the network processing device according to the current entry in the transmit memory;

means for transmitting data for the identified time slot period out from the identified current transmit channel register;

means for moving to a next entry in the transmit memory when the time slot period expires;

means for identifying a next time slot period and transmit channel register according to the next entry in the transmit memory; and

means for transmitting data out from the identified next transmit channel register for the identified next time slot period.

16. (Original) A system according to claim 15 including means for moving to a beginning entry in the transmit memory when a last entry is identified in the transmit memory and the time slot period expires.

17. (Original) A system according to claim 16 including means for waiting for a synchronization pulse before writing data into the transmit channel register identified by the beginning entry.

18. (Original) A system according to claim 15 including means for moving to a beginning entry in the transmit memory whenever a synchronization pulse is detected.

19. (Original) A system according to claim 15 including means for loading different entries into the receive memory and transmit memory according a TDM data stream format used for transmitting and receiving the data.

20. (Original) A system according to claim 15 including means for reading the receive memory and receiving data into the receive channel registers and reading the transmit memory and transmitting data out from the transmit channel registers at the same.

21. (Previously presented) ~~A computer readable medium for storing software for transferring data in a network processing device, comprising:~~ An apparatus comprising logic circuitry operable for:

~~code for~~ reading a current entry in a receive memory;

~~code for~~ identifying a time slot period for receiving the data according to the current entry in the receive memory;

~~code for~~ identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

~~code for~~ receiving data for the identified time slot period into the identified current receive channel register;

~~code for~~ moving the current entry to a next entry in the receive memory when the time slot period expires;

~~code for~~ identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

~~code for~~ receiving data into the identified next receive channel register for the identified next time slot period; and

~~code for~~ moving to a next entry in the receive memory according to a detected synchronization pulse.

22. (Original) ~~A computer readable medium~~ The apparatus according to claim 21 ~~including code~~ wherein the logic circuitry is further operable for moving to a beginning entry in the receive memory when a last entry is identified in the receive memory and the time slot period expires.

23. (Previously presented) A ~~computer readable medium for storing software for transferring data in a~~ network processing device~~, comprising~~ having logic circuitry for:

~~code for~~ reading a current entry in a receive memory;

~~code for~~ identifying a time slot period for receiving the data according to the current entry in the receive memory;

~~code for~~ identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

~~code for~~ receiving data for the identified time slot period into the identified current receive channel register;

~~code for~~ moving the current entry to a next entry in the receive memory when the time slot period expires;

~~code for~~ identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

~~code for~~ receiving data into the identified next receive channel register for the identified next time slot period; and

~~code for~~ waiting for a next synchronization pulse before shifting data into the receive channel register associated with the beginning entry.

24. (Previously presented) ~~A computer readable medium for storing software for transferring data in a~~ The logic circuitry in the network processing device ~~, comprising:~~ of claim 23 further configured for:

~~code for~~ reading a current entry in a receive memory;

~~code for~~ identifying a time slot period for receiving the data according to the current entry in the receive memory;

~~code for~~ identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

~~code for~~ receiving data for the identified time slot period into the identified current receive channel register;

~~code for~~ moving the current entry to a next entry in the receive memory when the time slot period expires;

~~code for~~ identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

~~code for~~ receiving data into the identified next receive channel register for the identified next time slot period; and

~~code for~~ moving to a beginning entry in the receive memory whenever a synchronization pulse is detected.

25. (Previously presented) A ~~computer readable medium for storing software for transferring data in a~~ network processing device~~, comprising~~ having logic circuitry configured for:

~~code for~~ reading a current entry in a receive memory;

~~code for~~ identifying a time slot period for receiving the data according to the current entry in the receive memory;

~~code for~~ identifying a current receive channel register in the network processing device to write the received data according to the current entry in the receive memory;

~~code for~~ receiving data for the identified time slot period into the identified current receive channel register;

~~code for~~ moving the current entry to a next entry in the receive memory when the time slot period expires;

~~code for~~ identifying a next time slot period and a next receive channel register according to the next entry in the receive memory;

~~code for~~ receiving data into the identified next receive channel register for the identified next time slot period;

~~code for~~ reading a current entry in a transmit memory;

~~code for~~ identifying a time slot period for transmitting the data according to the current entry in the transmit memory;

~~code for~~ identifying a current transmit channel register in the network processing device according to the current entry in the transmit memory;

~~code for~~ transmitting data for the identified time slot period out from the identified current transmit channel register;

~~code for~~ moving to a next entry in the transmit memory when the time slot period expires;

~~code for~~ identifying a next time slot period and transmit channel register according to the next entry in the transmit memory; and

~~code for~~ transmitting data out from the identified next transmit channel register for the identified next time slot period.

26. (Original) ~~A computer readable medium according to claim 25 including code~~ The logic circuitry in the network processing device of claim 25 further configured for moving to a beginning entry in the transmit memory when a last entry is identified in the transmit memory and the time slot period expires.

27. (Original) ~~A computer readable medium according to claim 26 including code~~ The logic circuitry in the network processing device of claim 26 further configured for waiting for a synchronization pulse before writing data into the transmit channel register identified by the beginning entry.

28. (Original) ~~A computer readable medium according to claim 25 including code~~ The logic circuitry in the network processing device of claim 25 further configured for moving to a beginning entry in the transmit memory whenever a synchronization pulse is detected.

29. (Original) ~~A computer readable medium according to claim 25 including code~~ The logic circuitry in the network processing device of claim 25 further configured for loading different entries into the receive memory and transmit memory according a TDM data stream format used for transmitting and receiving the data.

30. (Original) ~~A computer readable medium according to claim 25 including code~~ The logic circuitry in the network processing device of claim 25 further configured for reading the receive memory and receiving data into the receive channel registers and reading the transmit memory and transmitting data out from the transmit channel registers at the same.